AMENDMENTS TO THE CLAIMS:

Claims 1, 6, 7, 11 and 15 have been amended. Claims 17-20 have been added. Claim 4 has been previously canceled. This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) An integrated circuit interconnect structure, comprising:

a low K dielectric layer with an upper surface formed over a semiconductor;

a first trench formed in said low K dielectric layer wherein said trench has sidewalls;

a first contiguous barrier layer formed to a thickness X_1 over said upper surface of said low ~~k~~ K dielectric layer within said trench and formed to a thickness X_2 on said trench sidewalls wherein X_1 is greater than X_2, wherein the ratio X_1 to X_2 is greater than 3 to 2; and

copper formed over said first contiguous barrier.

2. (Original) The integrated circuit interconnect structure of claim 1 further comprising a second trench comprising sidewalls formed in said low K dielectric layer and separated from said first trench by a distance less than 160 nm.

3. (Original) The integrated circuit interconnect structure of claim 2 wherein said first contiguous barrier layer is formed to a thickness X_2 on said trench sidewalls of said second trench.

4. (Canceled).

5. (Original) The integrated circuit interconnect structure of claim 3 wherein the ratio X_1 to X_2 is greater than 3 to 2.

6. (Currently Amended) The integrated circuit interconnect structure of claim 1 further comprising a second contiguous barrier layer formed over said first contiguous barrier layer and beneath said copper.

7. (Currently Amended) A copper integrated circuit interconnect structure, comprising:

a low K dielectric layer with an upper surface formed over a semiconductor;

a plurality of trenches formed in said low K dielectric layer wherein said plurality of trenches has sidewalls;

a first contiguous barrier layer formed to a thickness X_1 over said upper surface of said low k K dielectric layer within said trench and formed to a thickness X_2 over said sidewalls of said plurality of trenches wherein the ratio of X_1 to X_2 is greater than 3 to 2; and

copper formed over said first contiguous barrier.

8. (Original) The integrated circuit interconnect structure of claim 7 wherein said plurality of trenches are separated from each other by a distance of less than 160 nm.

9. (Original) The integrated circuit interconnect structure of claim 7 further comprising a second contiguous barrier layer formed over said first contiguous barrier layer and beneath said copper.

10. (Original) The interconnect structure of claim 7 wherein the dielectric constant of the low K dielectric layer is less than or equal to approximately 3.7.

11. (Currently Amended) A method for forming a copper interconnect structure, comprising:

forming a low K dielectric layer with an upper surface over a semiconductor;

forming a plurality of trenches in said low K dielectric layer wherein said plurality of trenches has sidewalls;

forming a first contiguous barrier layer to a thickness X_1 over said upper surface of said low k K dielectric layer within said plurality of trenches and to a thickness X_2 over said sidewalls of said plurality of trenches wherein the ratio of X_1 to X_2 is greater than 3 to 2; and

forming copper over said first contiguous barrier.

12. (Original) The method of claim 11 wherein said plurality of trenches are separated from each other by a distance of less than 160 nm.

13. (Original) The method of claim 12 further comprising forming a second contiguous barrier layer over said first contiguous barrier layer and beneath said copper.

14. (Original) The method of claim 13 wherein the dielectric constant of the low K dielectric layer is less than or equal to approximately 3.7.

15. (Currently Amended) A method for forming an integrated circuit copper interconnect structure, comprising:

forming a low K dielectric layer with a dielectric constant less than or equal to approximately 3.7 with an upper surface over a semiconductor;

forming a plurality of trenches separated by a distance of less than 160 nm in said low K dielectric layer wherein said plurality of trenches has sidewalls;

forming a first contiguous barrier layer to a thickness X_1 over said upper surface of said low k K dielectric layer within said plurality of trenches and to a thickness X_2 over said sidewalls of said plurality of trenches wherein the ratio of X_1 to X_2 is greater than 3 to 2; and

forming copper over said first contiguous barrier.

16. (Original) The method of claim 15 further comprising forming a second contiguous barrier layer over said first contiguous barrier layer and beneath said copper.

17. (New) The integrated circuit interconnect structure of claim of claim 1 wherein controlled dielectric pore penetration includes one of a starving of reactants used to deposit the barrier layer and increasing a re-sputter component of barrier layer material, thereby reducing a penetration of reactants into the pores of said trench sidewalls.

18. (New) The integrated circuit interconnect structure of claim of claim 7 wherein controlled dielectric pore penetration includes one of a starving of reactants used to deposit the barrier layer and increasing a re-sputter component of barrier layer material, thereby reducing a penetration of reactants into the pores of said trench sidewalls.

19. (New) The method of claim of claim 11 wherein controlled dielectric pore penetration includes one of a starving of reactants used to deposit the barrier layer and increasing a re-sputter component of barrier layer material, thereby reducing a penetration of reactants into the pores of said trench sidewalls.

20. (New) The method of claim of claim 15 wherein controlled dielectric pore penetration includes one of a starving of reactants used to deposit the barrier layer and increasing a re-sputter component of barrier layer material, thereby reducing a penetration of reactants into the pores of said trench sidewalls.